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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,403	05/18/2005	Nobuo Kobayashi	123928	5897

25944 7590 08/29/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/535,403	KOBAYASHI, NOBUO	
	Examiner	Art Unit	
	Eduardo A. Rodela	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/18/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the reply filed June 13, 2006. It is acknowledged that claim 3 has been cancelled, and claims 1, 2, and 4-7 are still under consideration.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley et al. (US 6,946,676).

Regarding claim 1, Kelley et al. disclose in Figure 1, a field-effect transistor comprising:

a gate electrode [12] formed at one side a base substrate;

a source electrode [22] formed at the one side of the base substrate;

a drain electrode [24] formed at the one side of the base substrate [drain electrode 24];

an insulation layer [14] formed between the gate electrode and the source electrode and between the gate electrode and the drain electrode;

a semiconductor layer [18] formed around the source electrode and the drain electrode; and

a functional layer [16] provided so as to come into contact with the semiconductor layer [18] and containing electron acceptors [column 5, line 25 to column 6, line 25], said functional layer [16] being arranged between said semiconductor layer [18] and said insulating layer [12],

wherein electron acceptor is a pi-conjugate molecule composed of an ethylene molecule [column 5, line 25 to column 6, line 25, molecule is comprised of ethylene]. Although Kelley does not show the same structural orientation, many variations are well known in the art as shown by Kelley et al. (US 6,433,359) Figures 1-3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the OFET of Kelley oriented in one of several well known structural orientations for at least the purpose of designing a device which has electrodes that functionally meet the structural requirements of a specific terminal layout scheme.

Regarding claim 2, Kelley et al. disclose the field-effect transistor according claim 1. In addition, Kelley et al. disclose wherein the electron acceptor has a half-wave reduction potential -0.46 V or higher [column 5, line 25 to column 6, line 25, shows the electron acceptors as halogens, which satisfy the specified limitation].

Regarding claim 4, Kelley et al. discloses the field-effect transistor according to claim 1. In addition, Kelley et al. does specify the organic layer constituent details wherein the pi-conjugate structure has a carbon number of 3- to 15 and in which a heterocycle including an S atom as a heteroatom is formed [column 5, lines 25-35].

Regarding claim 5, Kelley et al. disclose in Figure 1, the field effect transistor according to claim 1. Kelley disclose wherein the functional layer has a thickness from about 5-400 nm [column 5, lines 10-18]. Kelley does not teach the thickness above 400 nm or below 5 nm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a functional layer of the specified thicknesses, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

Regarding claim 7, Kelley et al. disclose in Figure 1, a field-effect transistor comprising:

a gate electrode [12] formed at one side a base substrate;

a source electrode [22] formed at the one side of the base substrate;

a drain electrode [24] formed at the one side of the base substrate;

an insulation layer [14] formed between the gate electrode and the source electrode and between the gate electrode and the drain electrode;

a semiconductor layer [18] formed around the source electrode and the drain electrode; and

a functional layer [16] provided so as to come into contact with the semiconductor layer [18] and containing electron acceptors [column 5, line 25 to column 6, line 25], wherein the concentration of the electron acceptors contained in the functional layer is 0.01 to 10 mass percent [column 14, line 63 to column 15, line 20].]. Although Kelley does not show the same structural orientation, many variations are very

well known in the art as shown by Kelley et al. (US 6,433,359) Figures 1-3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the OFET of Kelley oriented in one of several well known structural orientations for at least the purpose of designing a device which has electrodes that functionally meet the structural requirements of a specific terminal layout scheme.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley et al. in view of Bai et al. (US 2004/0222412).

Regarding claim 6, Kelley et al. disclose the field effect transistor according to claim 1. Kelley et al. do not disclose the dimension for the insulating layer, wherein the functional layer satisfies the following expression (1); D2 * 0.001 =< d1 =< d2 * 1 ... (1), Where d1 denotes the thickness of the insulation layer. Bai et al. does disclose dimensions wherein the functional layer satisfies the following expression (1); D2 * 0.001 =< d1 =< d2 * 1 ... (1), Where d1 denotes the thickness of the insulation layer [Fig. 1: organic layer 18 and dielectric 16, paragraph 0044 discloses the dimensions of the dielectric layer, paragraph 0084 discloses the dimension of the dielectric layer, an almost satisfies the equation where 0.4 Angstroms =< 500 Angstroms =< 400 Angstroms]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kelley et al. with the teachings of Bai et al. and to further thin the gate dielectric so that the relative thicknesses of the organic layer be equal or larger than that of the dielectric layer. The ordinary artisan would have been motivated to do so in order to provide higher performance thin film transistors, since current flow is in the field effect transistor is inversely proportional to the gate dielectric thickness, so

the thinner the gate the faster the device. The examiner would like to note that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

Response to Arguments

Applicant's arguments with respect to the rejection(s) of claim(s) under Nishizawa have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kelley et al.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eduardo A. Rodela, Examiner

ER